AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A chip-scale package for photonic devices, comprising:

a window having one or more conductive traces on a first side of said window;

a chip fixed relative to the first side of said window;

a first housing extending around said chip and fixed relative to said window;

said chip having one or more electrical terminals;

said first housing having one or more electrical terminals; and

at least one terminal of said chip being bump bonded to a conductive trace on said window, and at least one terminal of said first housing being bump bonded to a conductive trace on said window.

2. (Original) The package of claim 1, wherein said chip is hermetically sealed by said window and said first housing.

3. (Original) The package of claim 2, wherein said first housing is sealed to said window at the periphery of said window by a sealing-type material.

4. (Cancelled)

5. (Previously Presented) The package of claim 1, wherein said chip comprises a photonic device.

6. (Cancelled)

7. (Previously Presented) The package of claim 5, further comprising a second housing situated adjacent to a second side of said window.

8. (Original) The package of claim 7, further comprising a ferrule having at least one optical fiber, which is placed adjacent said second side of said window.

9. (Original) The package of claim 8, further comprising a lens formed on or in said window.

10. (Original) The package of claim 9, wherein said ferrule is accepted by an opening in said second housing.

11. (Original) The package of claim 10, wherein an end of said optical fiber is proximate to said window so that light from the fiber can go through the optical fiber and said window to the photonic device, and/or so that light from the photonic device can go through said window and the least one optical fiber.

12.- 17. (Cancelled)

18. (Withdrawn) The package of claim 17, further comprising a ferrule having at least one optical waveguide.

19. (Withdrawn) The package of claim 18, wherein said ferrule plugs into a portion of said second housing.

20. (Withdrawn) The package of claim 19, wherein the at least one optical waveguide becomes aligned with the at least one photonic device when said ferrule is plugged into the portion of said second housing.

21. (Withdrawn) The package of claim 20, further comprising a pin for holding said ferrule in a plugged-in position in the portion of said second housing.

22. (Withdrawn) The package of claim 21, wherein said window has at least one lens situated between the at least one photonic device and the at least one optical waveguide.

23. (Withdrawn) The package of claim 22, wherein the at least one optical waveguide is an optical fiber.

24. - 27. (Cancelled)

28. (Withdrawn) The package of claim 27, further comprising a plug having an at least one optical waveguide, wherein said plug fits into said second housing and is aligned with the at least one alignment feature such that one end of the at least one optical waveguide is proximate to said window.

29. (Withdrawn) The package of claim 28, wherein the one end of the at least one optical waveguide is aligned with the at least one photonic device.

30. (Withdrawn) The package of claim 29, further comprising at least one pin securing said plug in said second housing.

31. (Withdrawn) The package of claim 28, wherein the at least one photonic device is a VCSEL.

32. (Withdrawn) The package of claim 29, wherein:
said first housing is composed of ceramic; and
said window is composed of quartz.

33. (Previously Presented) A chip-scale package for electronic devices, comprising:

a transparent window having at least one conductive trace patterned on a surface of said window;

a semiconductor chip fixed relative to said window having at least one terminal connected to the at least one conductive trace;

a first housing surrounding said chip and affixed to said window; and

a conductive path from the at least one conductive trace to an at least one pad on an external surface of said enclosure.

34. (Original) The package of claim 33, wherein said chip comprises a photonic device.

35. (Original) The package of claim 34, wherein said window has at least one feature on the surface of said window for alignment.

36. (Original) The package of claim 34, wherein the conductive path is partially embedded in said first housing.

37. (Original) The package of claim 36, wherein the conductive path is connected on one end to a pad on the external surface of said first housing.

38. (Original) The package of claim 37, wherein said conductive path is connected on another end to another pad which is connected to the at least one said conductive trace on said window.

39. (Original) The package of claim 38, wherein said first housing is sealed to said window at a periphery of said window.

40. (Original) The package of claim 39, wherein said first housing is sealed to said window at the periphery of said window by a solder-type material.

41. (Original) The package of claim 39, wherein said first housing is sealed to said window at the periphery of said window by an adhesive-type material.

42. (Original) The package of claim 39, wherein said chip is hermetically sealed by said window and said first housing.

43. (Original) The package of claim 39, wherein said chip is environmentally sealed by said window and said first housing.

44. (Original) The package of claim 42, wherein said window has at least one refractive optical element on the surface of said window.

45. (Original) The package of claim 43, wherein said window has at least one refractive optical element on the surface of said window.

46. (Original) The package of claim 42, wherein said window has at least one diffractive optical element on the surface of said window.

47. (Original) The package of claim 43, wherein said window has at least one diffractive optical element on the surface of said window.

48. (Original) The package of claim 35, further comprising a second housing attached to said first housing.

49. (Original) The package of claim 48, wherein said second housing is mechanically registered to said first housing by the at least one feature on the surface of said window.

50. (Original) The package of claim 49, further comprising a ferrule having at least one optical waveguide.

51. (Original) The package of claim 50, wherein the at least one optical waveguide is proximate to said window so that light from the waveguide can pass through said window to the at least one photonic device, and/or so that light from the photonic device can go through said window and to the at least one optical waveguide.

52. (Original) The package of claim 51, wherein said window has at least one lens situated between the at least one photonic device and said at least one optical waveguide.

53. (Original) The package of claim 52, wherein the at least one optical waveguide is an optical fiber.

54. (Original) The package of claim 51, further comprising at least one pin securing said ferrule to said first housing.

55. (Original) The package of claim 34, wherein the at least one photonic device is a VCSEL.

56. (Original) The package of claim 33, wherein said first housing comprises ceramic.

57. (Original) The package of claim 33, wherein said window comprises quartz.

58. (Previously Presented) The package of claim 1, wherein the at least one terminal of said chip is bump bonded to the same conductive trace as the at least one terminal of said first housing.

59. (Previously Presented) The package of claim 1, wherein the at least one terminal of said first housing is electrically connected to a terminal outside of said first housing.

60. (Previously Presented) The package of claim 59, wherein said first housing is a multi-layer housing, and the at least one terminal of said first housing is electrically connected to a terminal outside of said first housing via a trace in the multi-layer housing.

61. (Previously Presented) The package of claim 60, wherein said chip includes a back side facing away from said window, wherein the back side of said chip is electrically connected to a terminal outside of said first housing via another trace in the multi-layer housing.

62. (Previously Presented) A chip-scale package for photonic devices, comprising:

a window;

a chip fixed relative to a first side of said window;

a first housing having a body with an outer surface and an inner surface, the inner surface extending around said chip and fixed relative to said window to form a chip cavity;

said first housing having at least one electrical terminal along its outer surface, which is electrically connected through the body of the first housing to at least one electrical terminal along the inner surface of the first housing;

said window includes one or more conductive traces;

said chip includes one or more electrical terminals; and

at least one terminal of said chip is bump bonded to a conductive trace on said window, and at least one terminal along the inner surface of the first housing is bump bonded to a conductive trace on said window.

63. (Cancelled)

64. (Previously Presented) The package of claim 62, wherein the at least one terminal of said chip is bump bonded to the same conductive trace as the at least one terminal of said first housing.

65. (Previously Presented) The package of claim 62, wherein said first housing is a multi-layer housing.

66. – 68. (Cancelled)